

CLIPPER, CLAMPER AND VOLTAGE MULTIPLIER

Clippers

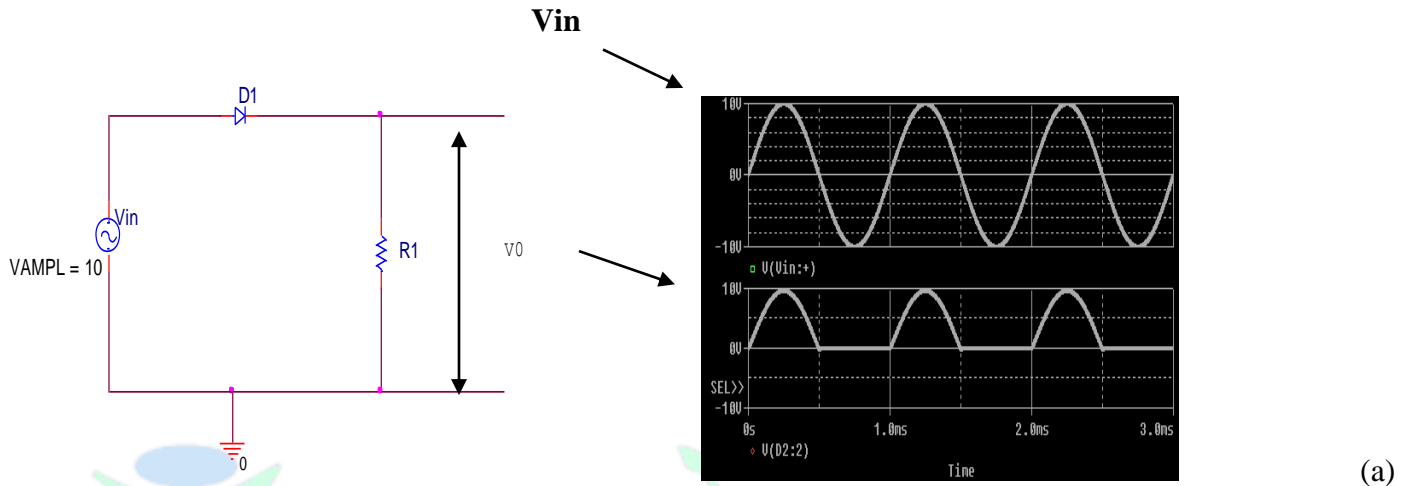
Clippers are those diode circuits that have the ability to clip off (i.e., remove) a portion of input wave that lies below or above a specified level, without distorting its remaining part. This type of processing is useful for signal shaping, circuit protection, and communications. The half wave rectifier is the simplest form of diode clipper.

There are two general categories of clippers: series and parallel. In the series clipper the diode and the load are in series, while in the parallel clippers the diode is in parallel to the load. Further, each of these two categories has two types: negative and positive.

Series Clipper: Figure (1) shows series negative clipper. For negative input voltages, the diode is reverse biased. It behaves as an open switch. Therefore, the output V_o is zero. For positive input voltage, the diode is forward biased. It now behaves as a closed switch, and the output V_o becomes same as the input V_{in} . When a sinusoidal voltage of peak value V_m (here $V_m=10V$) is applied to its input, negative half is clipped off and the positive half appears as it is in the output, as shown in Fig.1(b).

Guidelines to Solve a Clipper Circuit:

1. Based on the direction of the diode, find the polarity of the applied voltage that is likely to make the diode in 'OFF' state and in 'ON' state.
2. Determine the value of the applied voltage that will cause a change in the state of the diode from 'OFF' to 'ON'. This is the transition level.
3. With diode 'ON', determine the relation between the output V_o and the input V_{in} .
4. Plot the waveshape of the output V_o for the given waveshape of the input V_{in} .



(b)

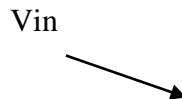
Fig. 1: Series Negative Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} > 0$; D1 is on; $V_o = V_{in}$.

For $V_{in} < 0$; D1 is off; $V_o = 0$

Series Positive Clipper: By reversing the terminals of the diode in the circuit of Fig. 1(a), we get a series positive clipper as shown in Fig. 2. Now the diode is short only when the input is negative, When the input is positive, the diode is in open circuit state. As a result, the output is zero. As shown in fig, 2(b), the output has its positive half clipped off.



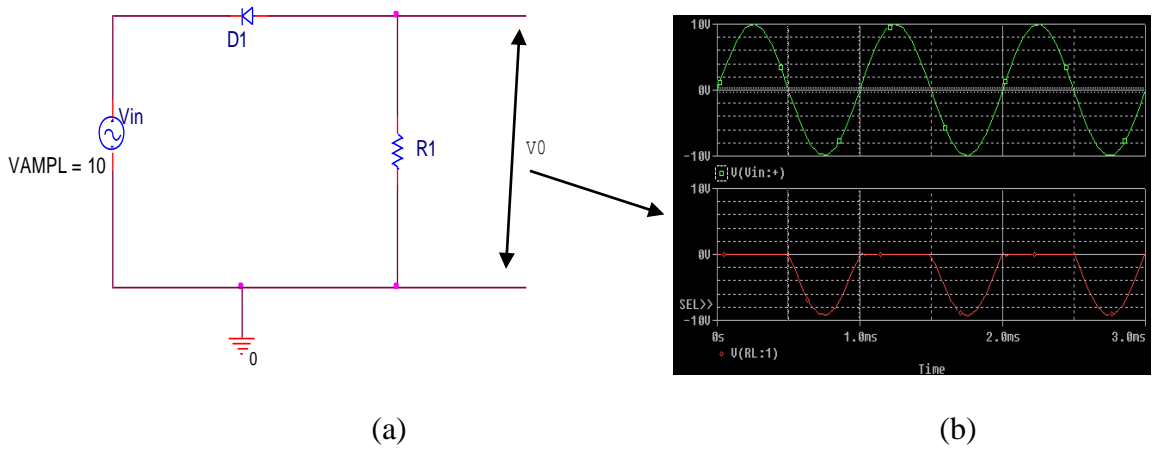


Fig. 2: Series Positive Clipper (a) Circuit (b) Input- output waveform

Working:

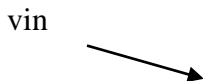
For $V_{in} > 0$; D1 is off; $V_o = 0$

For $V_{in} < 0$; D1 is on; $V_o = V_{in}$

Series Biased Clippers:

The term bias means applying an external voltage to change the dc level of a circuit. Example 1, 2, 3 and 4 shows different series biased clipper circuits along with their input output waveforms and working.

Example.1



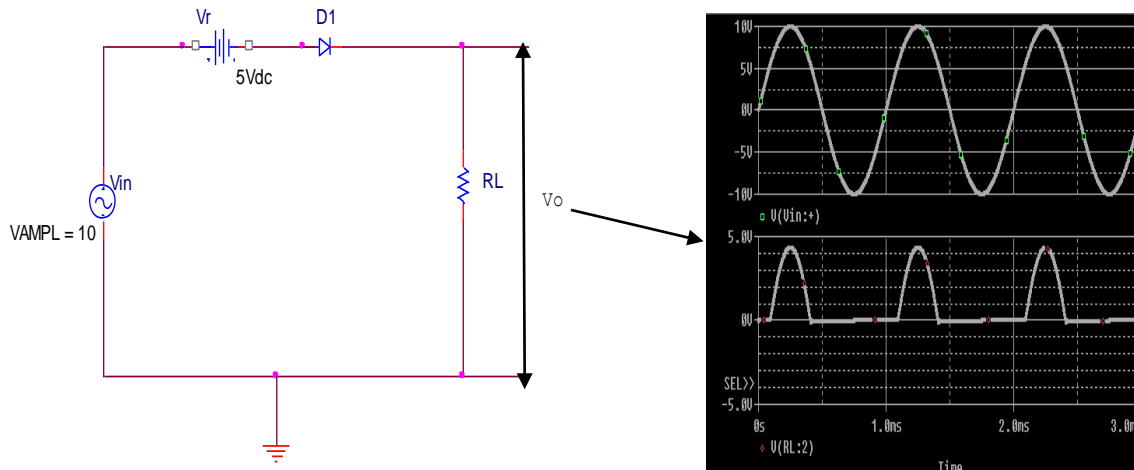


fig. 3: Series Positive Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} - 5 > 0$ or $V_{in} > 5V$; D1 is on; $V_o = (V_{in} - 5)$

For $V_{in} - 5 < 0$ or $V_{in} < 5V$; D is off; $V_o = 0$

Example 2

Vin

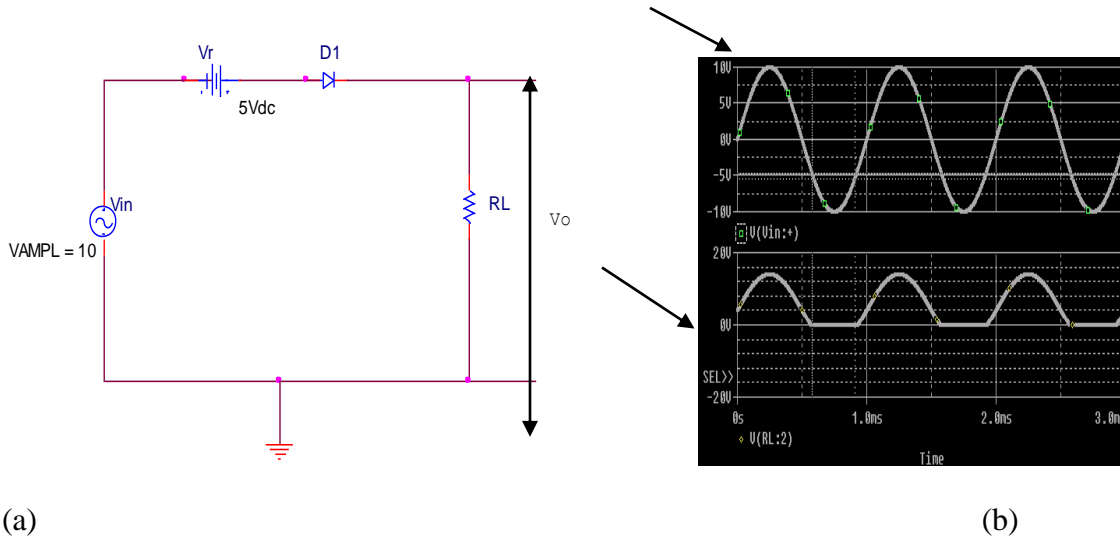


Fig. 4: Series Negative Clipper (a) Circuit (b) Input- output waveform

Working

For $V_{in} + 5 > 0$ or $V_{in} > -5V$; D1 is on; $V_o = (V_{in} + 5)$

For $V_{in} + 5 < 0$ or $V_{in} < -5V$; D1 is off; $V_o = 0$

Example.3

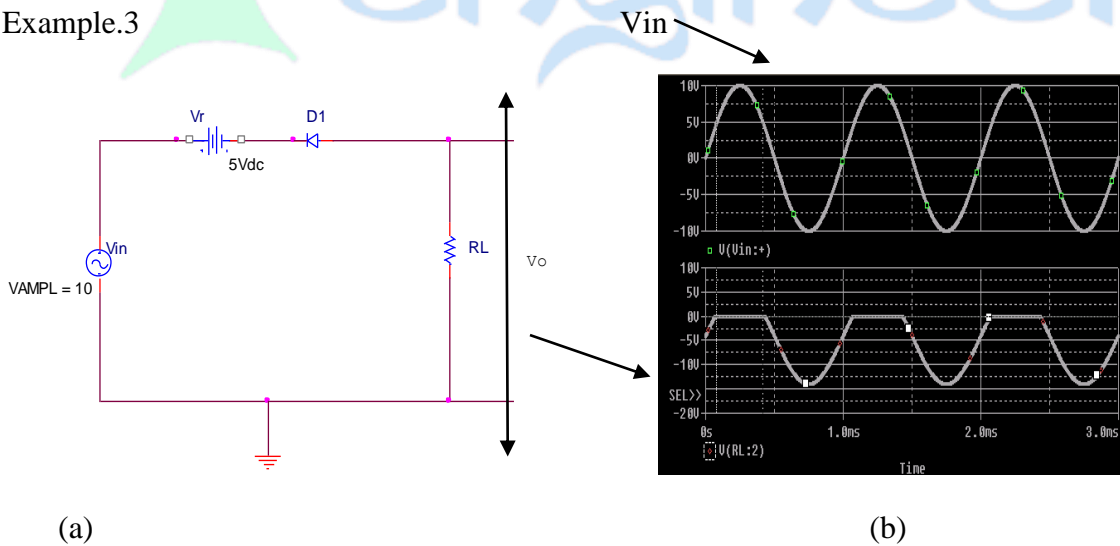


Fig. 5: Series Positive Clipper (a) Circuit (b) Input- output waveform

Working

For $V_{in}-5 < 0$ or $V_{in} < 5V$; D1 is on; $V_o = (V_{in}-5)$

For $V_{in}-5 > 0$ or $V_{in} > 5V$; D1 is off; $V_o = 0$

Example. 4

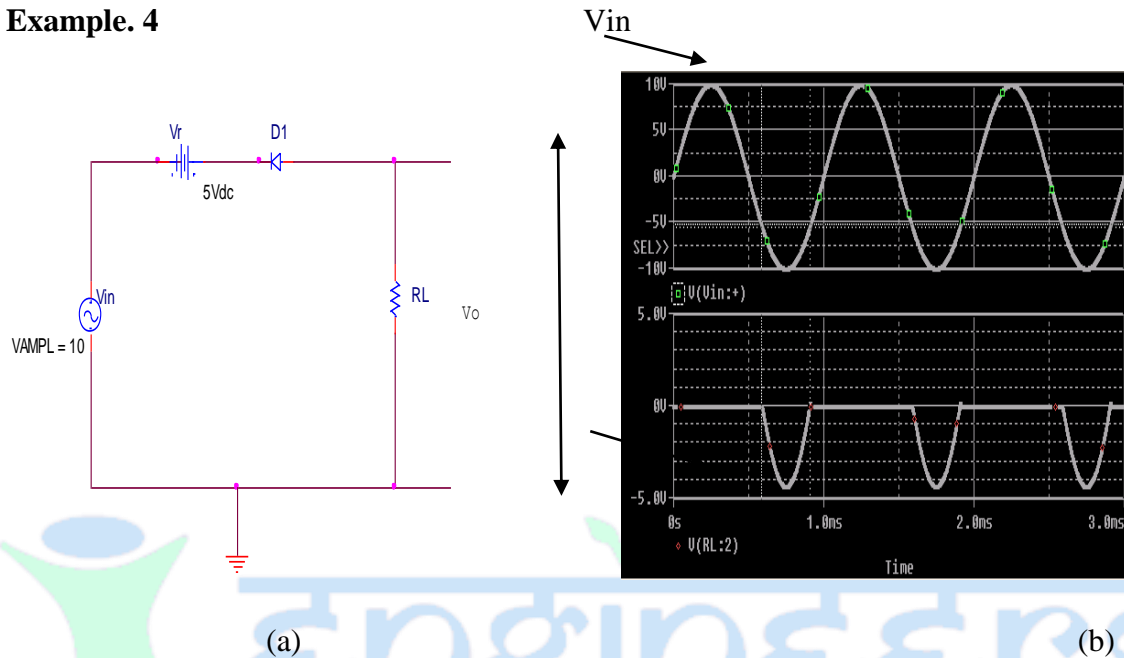


Fig 6: Series Positive Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in}+5 < 0$ or $V_{in} < -5V$; D1 is on; $V_o = (V_{in}+5)$

For $V_{in}+5 > 0$ or $V_{in} > -5V$; D1 is off; $V_o = 0$

Parallel Clipper: Fig. (7) shows the circuit of a parallel clipper circuit. During the positive half cycle of the input signal, the diode turns 'off'. It becomes an open circuit, so the input signal is obtained at the output. During negative half cycle of the input, The diode turns 'on'. It behaves as short circuit across the output terminals. So the output voltage is zero. Examples 5-9 shows different shunt clipper circuits with applied bias along with input output waveforms and working.

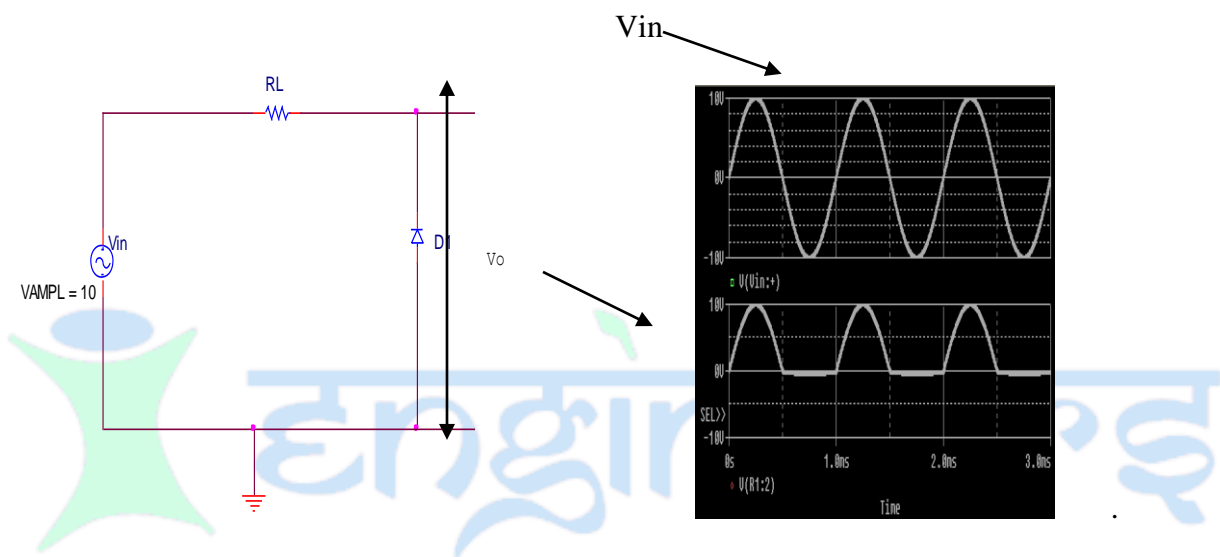


Fig 7: Shunt Negative Clipper (a) Circuit (b) Input - output waveform

Working:

For $V_{in} > 0$; D1 is off; $V_o = V_{in}$

For $V_{in} < 0$; D1 is on; $V_o = 0$

Example 5

V_{in} →

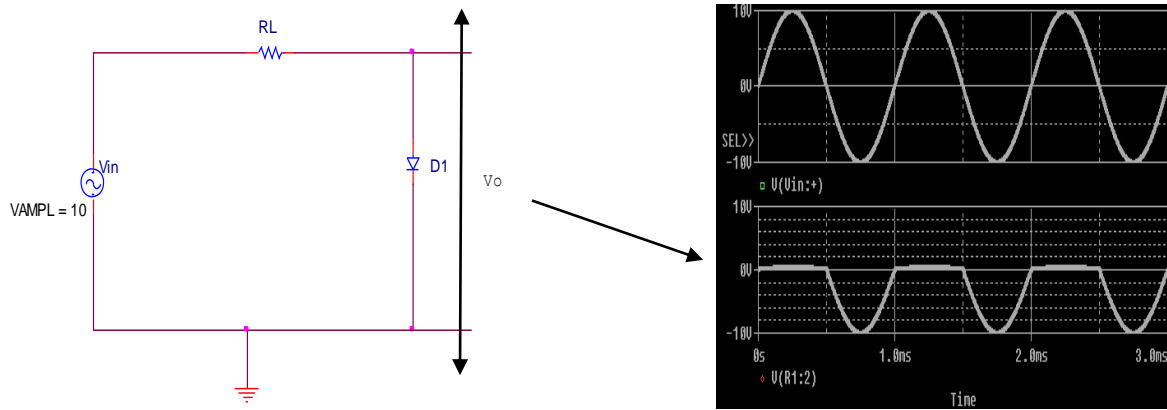


Fig 8: Shunt Positive Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} > 0$; D1 is on; $V_o = 0$

For $V_{in} < 0$; D1 is off; $V_o = V_{in}$

Example 6

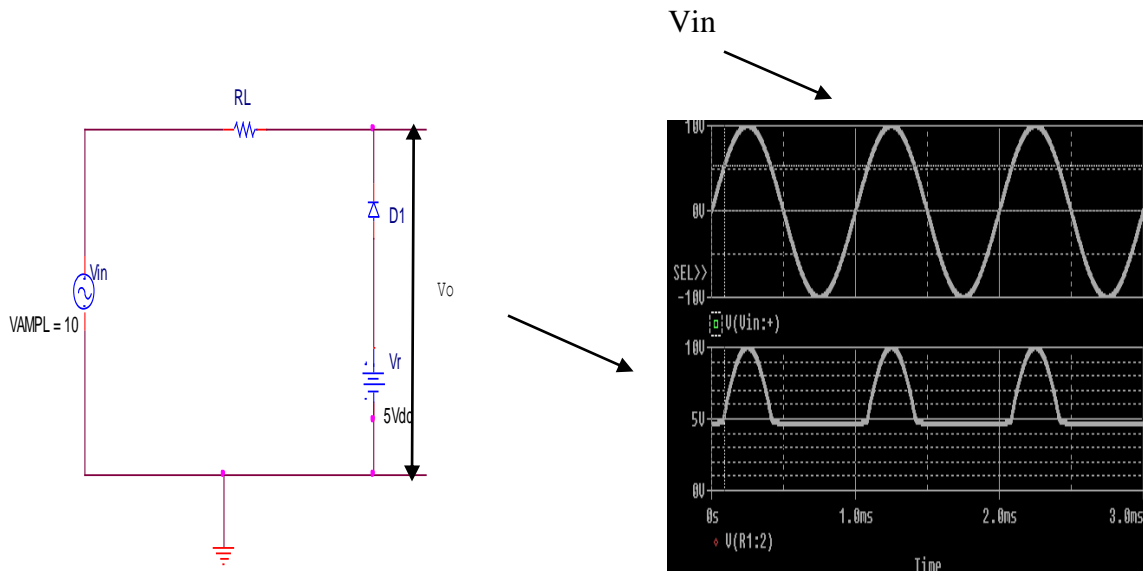


Fig 9: Shunt Negative Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} < -5V$; D1 is on; $V_o = 5V$

For $V_{in} > -5V$; D1 is off; $V_o = V_{in}$

Example 7

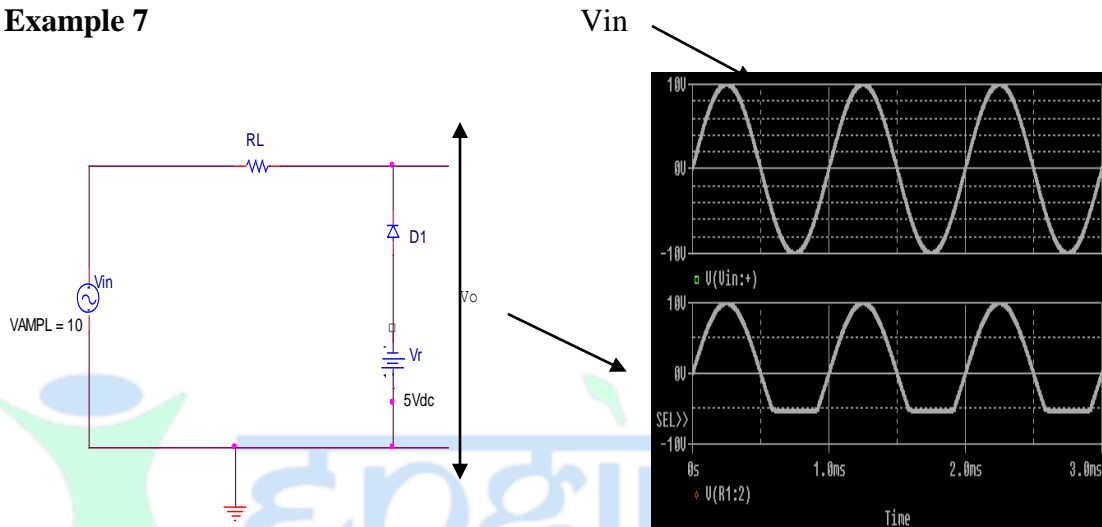


Fig 10: Shunt Negative Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} < -5V$; D1 is on; $V_o = -5V$

For $V_{in} > -5V$; D1 is off; $V_o = V_{in}$

Example 8

Vin

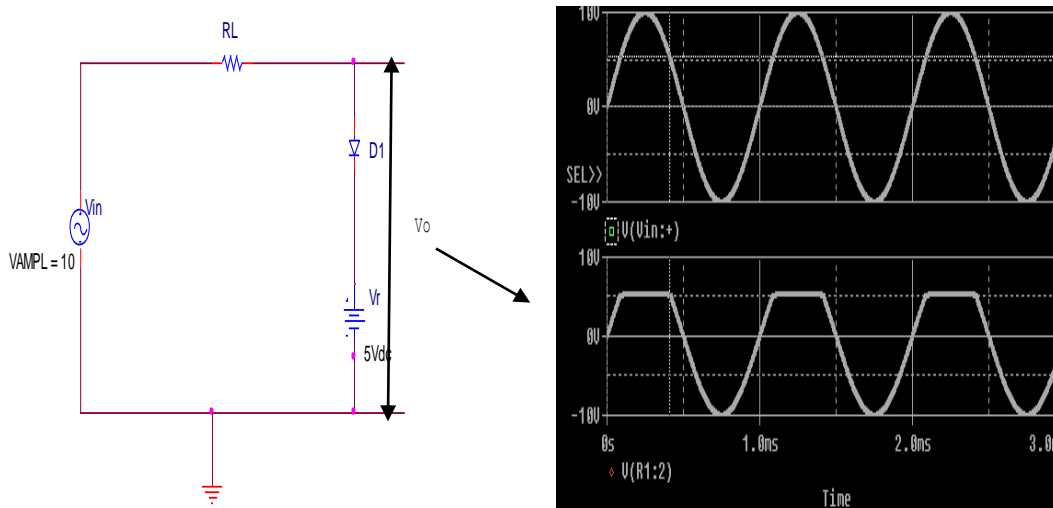


Fig 11: Shunt Positive Clipper (a) Circuit (b) Input- output waveform

Working:

For $V_{in} - 5 > 0$ or $V_{in} > 5V$; D1 is on; $V_o = 5V$

For $V_{in} - 5 < 0$ or $V_{in} < 5V$; D1 is off; $V_o = V_{in}$

Example 9

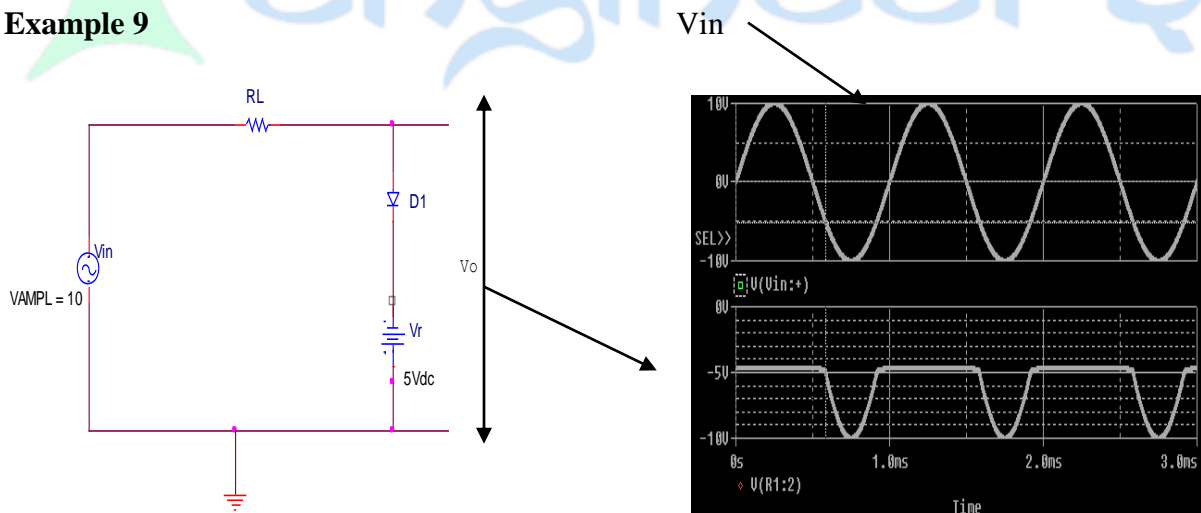


Fig 12: Shunt Positive Clipper (a) Circuit (b) Input- output waveform

Working:

$V_{in} + 5 > 0$ or $V_{in} > -5V$; D1 is on; $V_0 = -5V$

$V_{in} + 5 < 0$ or $V_{in} < -5V$; D1 is off; $V_0 = V_{in}$

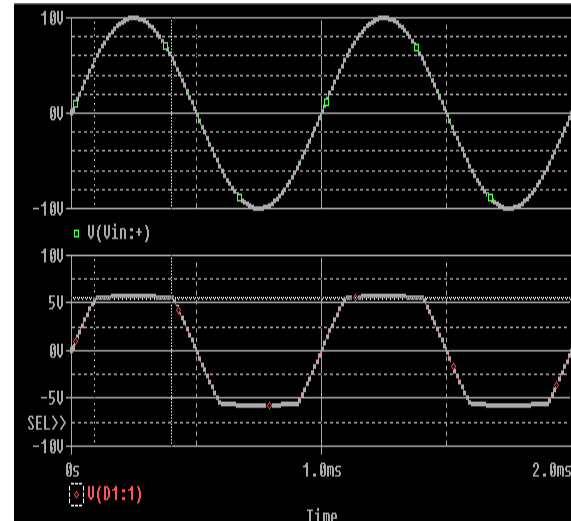
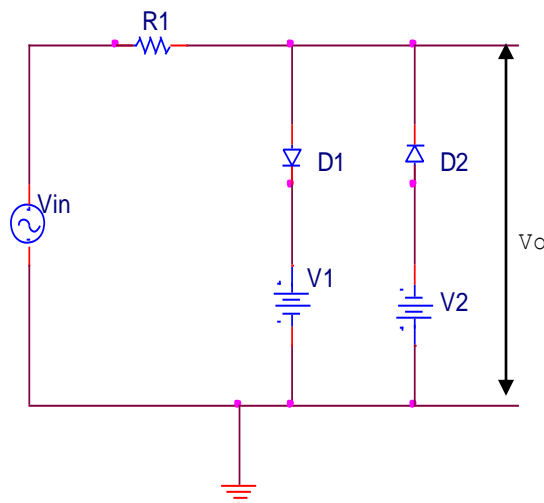


Fig 13: Combination Clipper (a) Circuit (b) Input- output waveform

Clamper

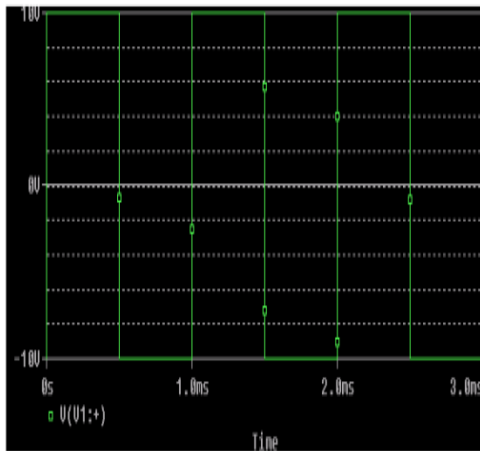
A clamper clamps (or shifts) either the positive peak or the negative peak of a signal to a definite level without distorting the waveform. A clamper circuit must have a diode, a capacitor, and a resistor. In addition, it can also have an additional dc supply to introduce an additional shift. The time constant $\tau = RC$ is made much larger than the period T of the signal. This ensures that the capacitor does not significantly discharge during the interval when the diode is not conducting. A clamper can be either a positive or a negative clamper.

Positive Clamper:

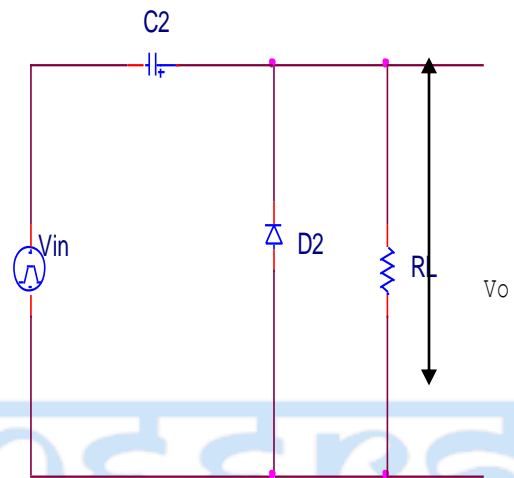
Fig. 1 shows a simple positive clamper. The input is a square wave. The capacitor is initially uncharged. On the first negative half cycle of the input voltage, the diode turns 'on'. The capacitor starts charging. The voltage across capacitor become V_m (peak value of the input) with the polarity as shown. During the positive half cycle the diode turns 'off'. The capacitor

tends to discharge through resistance R. However the time constant $\tau=RC$ has been made much larger than the period T of the input. Hence the capacitor remains almost fully charged during the ‘off’ time of the diode. The capacitor acts like a battery of V_m volts. Applying KVL in counterclockwise direction in the outer loop, we get

$$V_o - V_m - V_i = 0 \quad \text{or} \quad V_o = V_m + V_i$$



Input Waveform



Clamper circuit

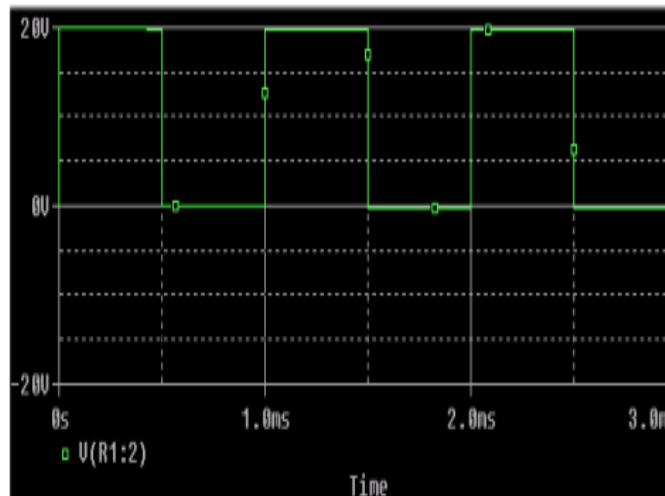
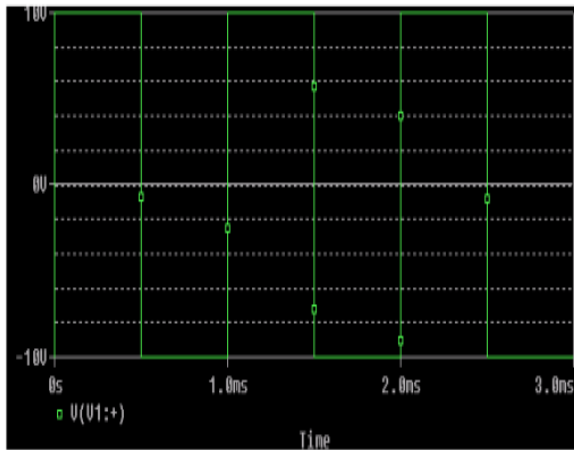


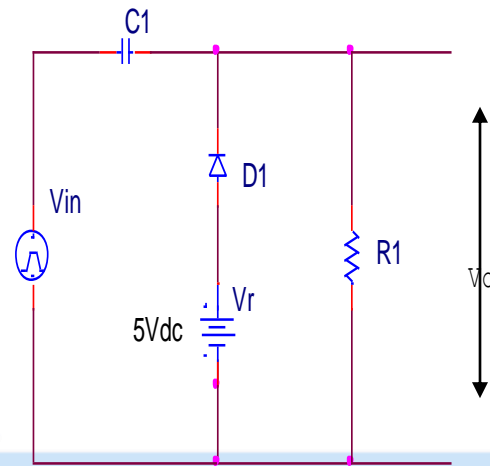
Fig. 1 O toutput waveform across AB

Positive Clamper With Applied Bias

Fig.(2) and **(3)** shows positive clamper circuits with applied bias. In **fig.(2)** the capacitor charges up to V_m+V_r during the negative half cycle of the input signal. In the positive half cycle, capacitor holds this voltage, so $V_o=V_{in}+V_m+V_r$.



Input Waveform



Clamper circuit

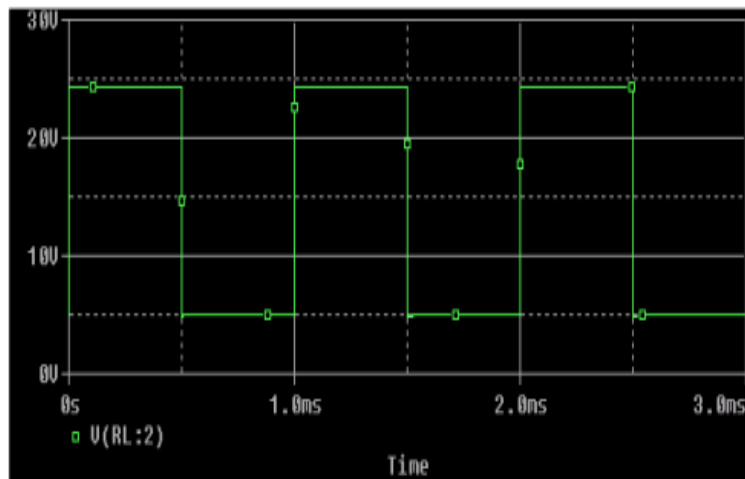
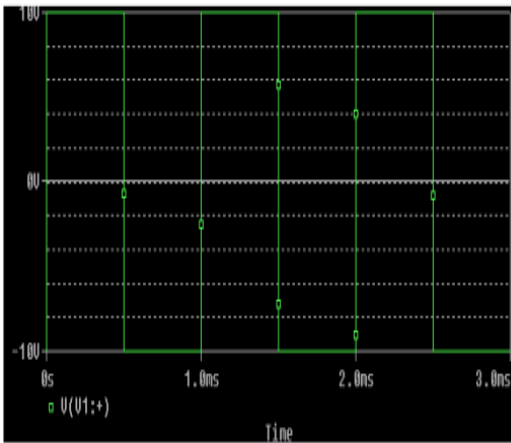
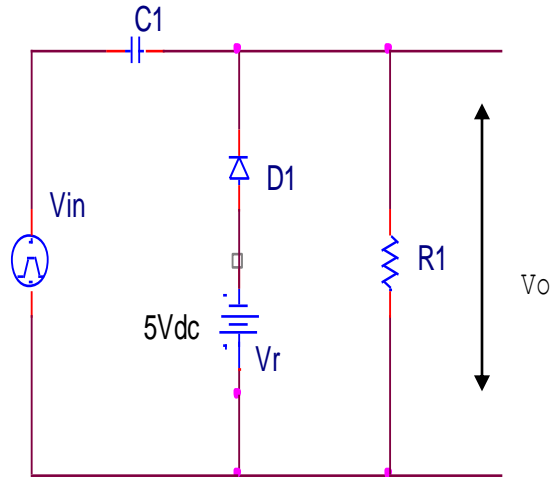


Fig. 2 Ooutput waveform

In **fig.(3)** the capacitor charges up to $V_m - V_r$ during the negative half cycle of the input signal. In the positive half cycle, capacitor holds this voltage, so $V_o = V_{in} + V_m - V_r$.



Input Waveform



Clamper circuit

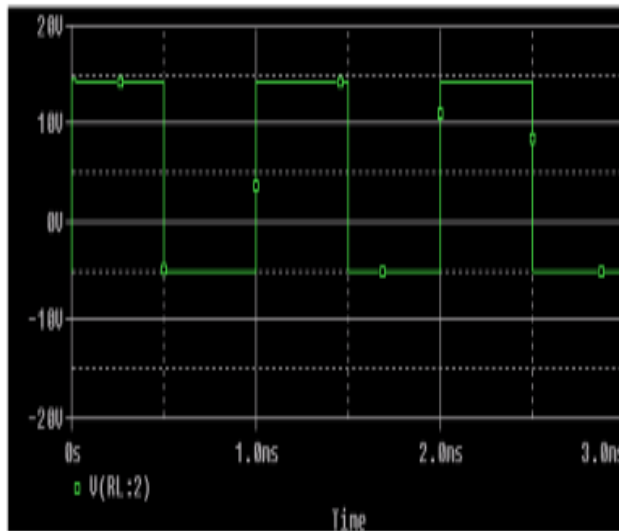
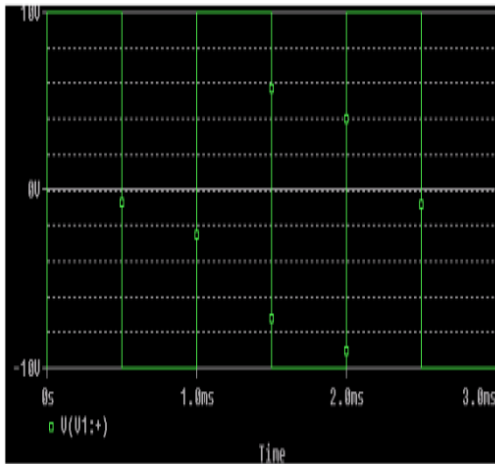


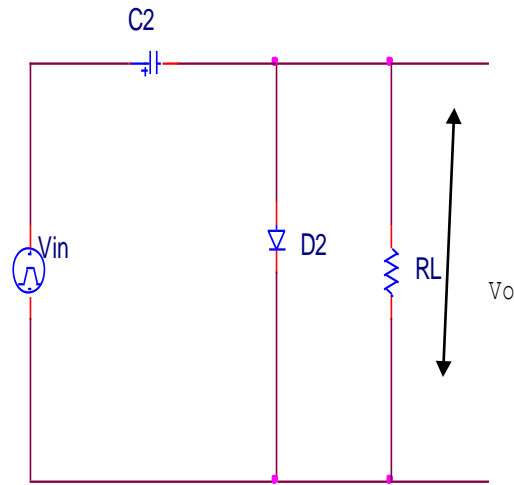
Fig. 3 Output waveform

Negative Clamper:

If we turn around the diode of **fig.(1)**, we get a negative clamper as in **fig.(4)**. Now the capacitor charges during positive half cycle of the input upto V_m , with the polarity as shown in **fig(4)**. During negative half cycle of the input the capacitor holds this voltage and hence the output $V_o = V_{in} - V_m$



Input Waveform



Clamper circuit

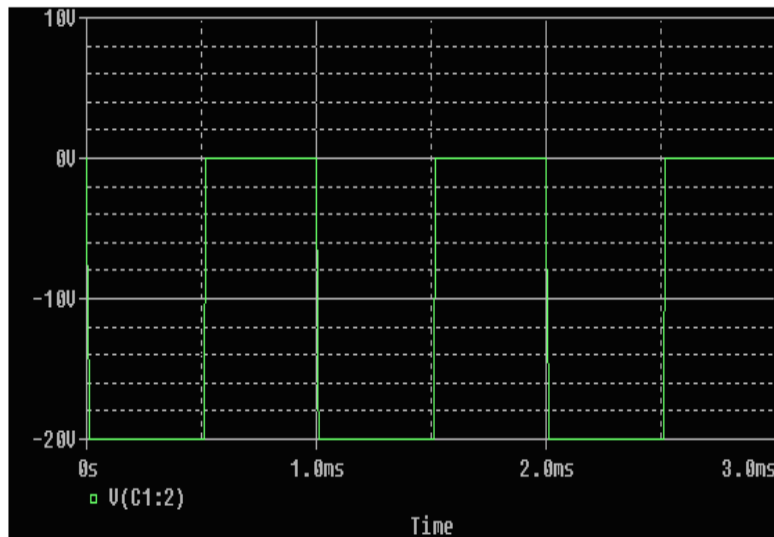
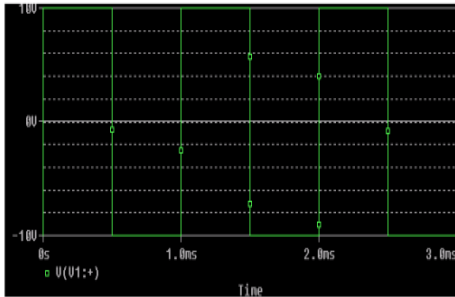
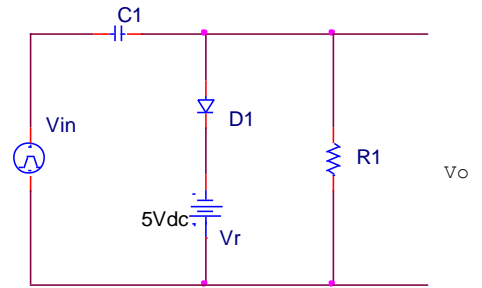


Fig. 4 Output waveform

Negative Clamper With Applied Bias: **Fig. (5) and (6)** shows the negative clamper circuits with applied bias. In **fig.(5)** the capacitor charges up to $V_m + V_r$. During negative half cycle, capacitor voltage remains constant and hence $V_o = V_{in} - V_m - V_r$



Input waveform



Clamper circuit

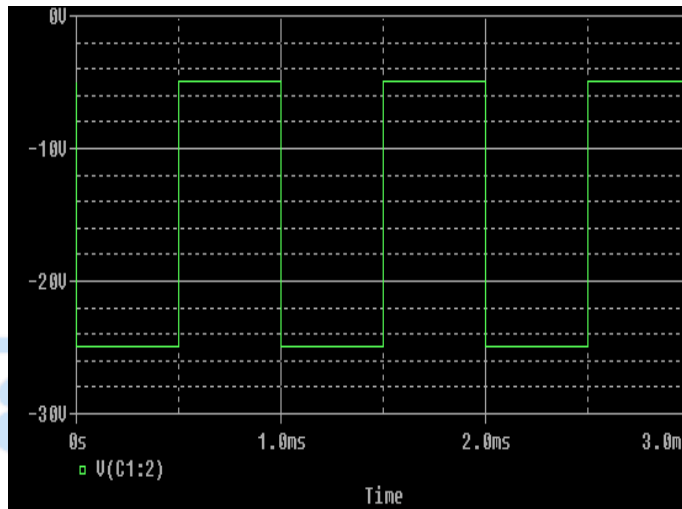
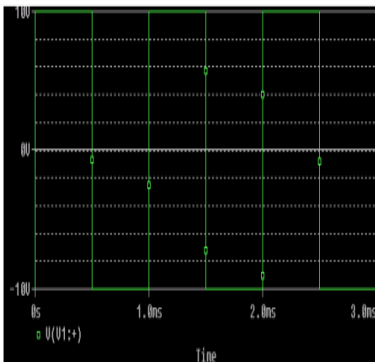
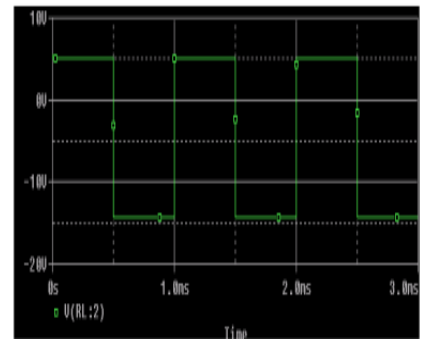
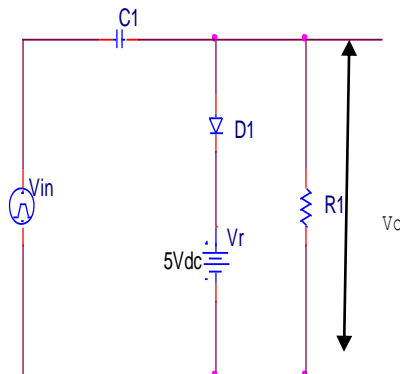


Fig. 5 Output waveform

In **fig.(6)** the capacitor charges up to $V_m - V_r$. During negative half cycle, capacitor voltage remains constant and hence $V_o = V_{in} - V_m + V_r$



Input Waveform



Output waveform

Fig. 6

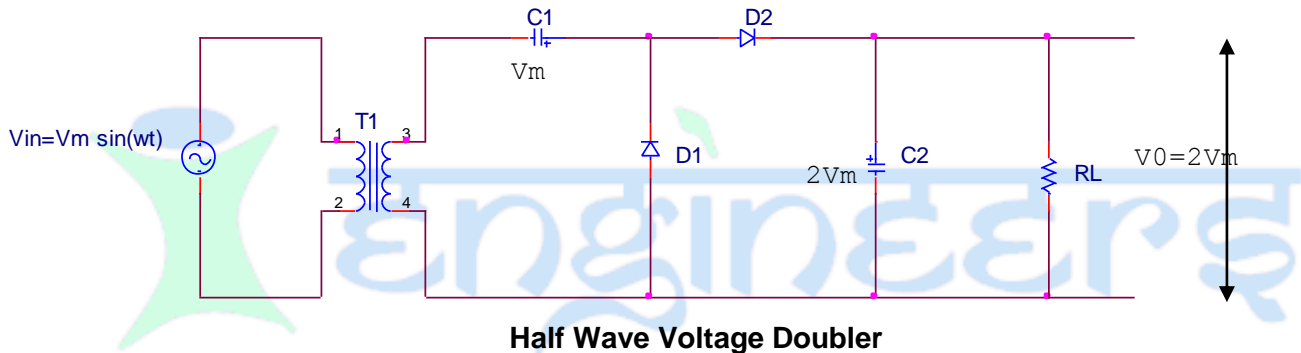
Voltage Multipliers: A voltage multiplier is a new kind of power supply. It uses a transformer of relatively low peak voltage and steps up the peak output voltage to two, three, four or more times the peak rectified voltage.

Half Wave Voltage Doubler: Fig. 7(a) shows the circuit of a half wave voltage doubler. It is in fact a combination of two circuits-a positive clamper and a half wave rectifier with shunt capacitor filter.

Working: During the negative half cycle of the of the input signal, diode D1 conducts (and diode D2 is cut off), Assuming ideal diodes D1 behaves as short circuit and capacitor C1 is charged up to peak input voltage (V_m) as shown in fig.(7(b)). During the positive half cycle of the input diode D1 is cut off and D2 conducts. Now, we can sum the voltage around the outside loop as shown in fig. 7(c),

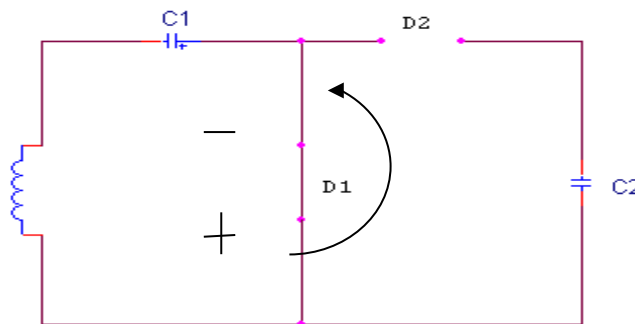
$$-V_{c2} + V_m + V_{c1} = 0 \quad \text{or} \quad -V_{c2} + V_m + V_m = 0 \quad \text{or} \quad V_{c2} = 2V_m$$

On the next negative half cycle, D2 is nonconducting and capacitor C_2 will discharge through load resistance r_L . If no load is connected across C_2 , both capacitors stay charged- C_1 to V_m and C_2 to $2V_m$.



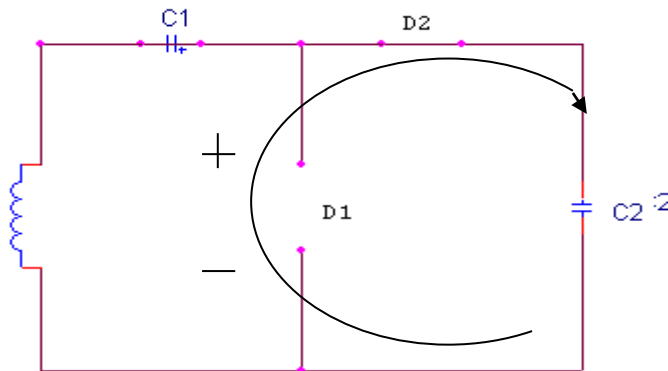
Half Wave Voltage Doubler

Fig.7 (a)



During Negative half cycle

Fig.7 (b)

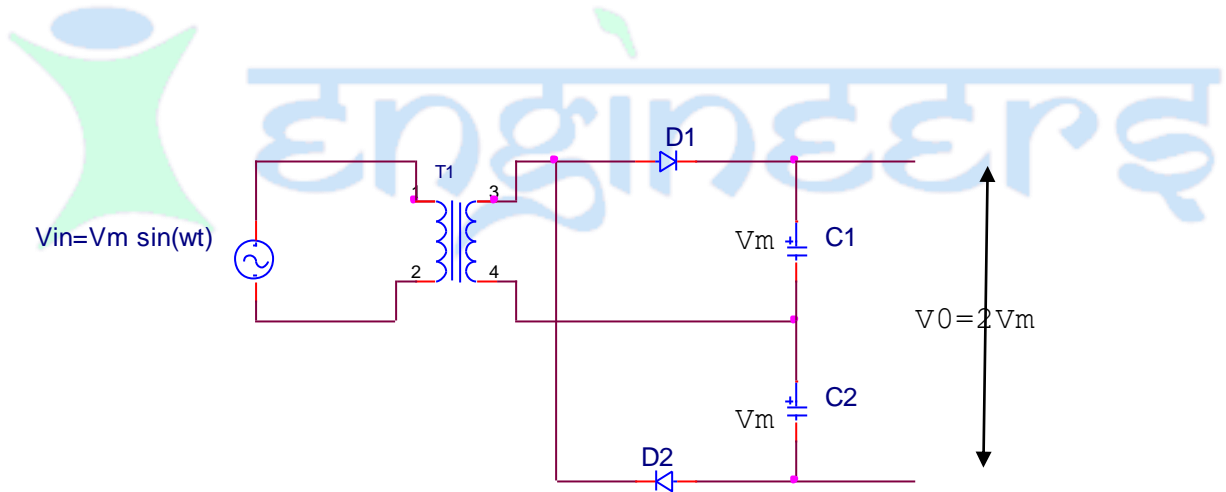


During Positive half cycle

Fig.7 (c)

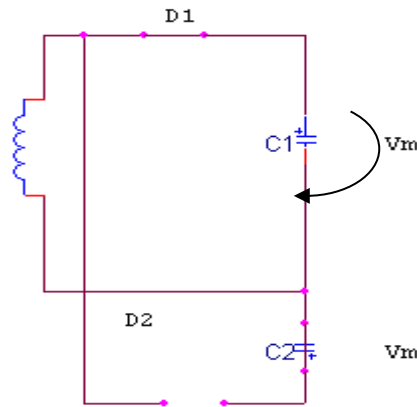
Full Wave Voltage Doubler: Fig.8(a) shows the circuit of a full wave voltage doubler. During the positive half cycle shown in fig.8(b), D1 conducts and D2 is cut off. In this cycle C1 charges up to peak voltage V_m .

During the negative half cycle shown in fig.8(c), D2 conducts and D1 is cut off. In this cycle C2 charges up to p peak voltage V_m . The total voltage across C1 & C2 gives the output as $2V_m$.



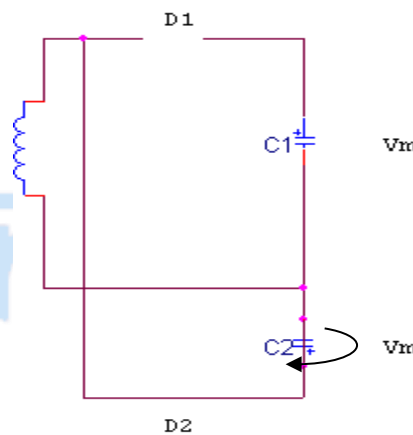
Full Wave Voltage Doubler

Fig.8(a)



Full Wave Voltage Doubler: During Positive Half Cycle

Fig.8(b)



Full Wave Voltage Doubler: During Negative Half Cycle

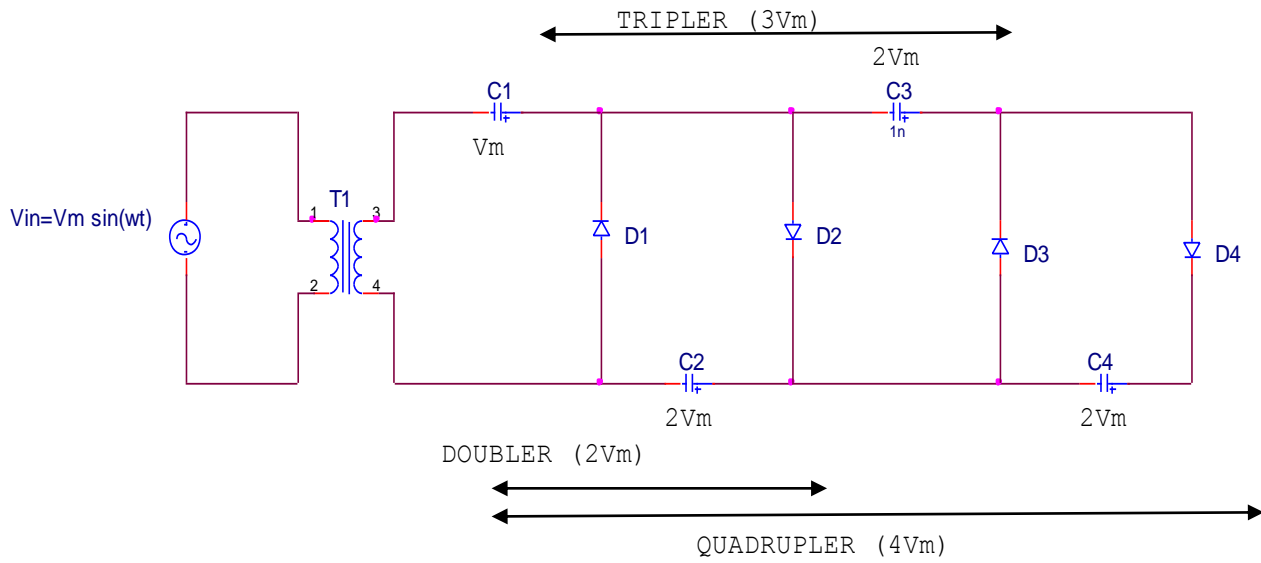
Fig.8(c)

Voltage Tripler and Quadrupler: Fig. 9 shows an extension of half wave voltage doubler. This circuit can three and four times the peak input voltage. From the pattern of the circuit, it is obvious that more sections of diodes and capacitors we can get output voltage which may be five, six, seven and so on, of the peak input voltage.

Working: During first negative half cycle, C1 charges through D to peak input V_m , next in the positive half cycle, C2 charges through d2 to $2V_m$, developed by the sum of the voltages across C1 and the input.

During next negative half cycle, D3 conducts and the voltage across charge up to $2V_m$ which is sum of input and voltage across C1. In the positive half cycle, D2 and D4 conduct, Now C3 acts as a battery of $2V_m$ voltage, thereby charging the capacitor C4 to $2V_m$.

As shown in fig., the voltage across C2 is $2V_m$, across C1 & C3 it is $3V_m$, & across C2 & C4 it is $4V_m$.



Voltage Tripler and Quadrupler

Fig.9



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